Team sdmay22-14

Project Title: RISC-V SoC Hardware Vulnerability Detection Toolset

Date: 10/24/2021

Members:

- Mason Korkowski -

- Micah Mundy -

- Gerald Edeh -

- Kolton Keller -

-Eva Kohl -

- Savva Zeglin -

- Magnus Anderson -

What we've accomplished in the past week/what we've been researching

- Mason Korkowski - Continued finding Verilog and System verilog linters, Currently looking at SVLint as it is open sourced and fairly simple so adding custom Lint cases may be possible. Additionally it should be able to look at different structures as well.

- Micah Mundy - Injecting bugs in the 2021 SoC and attempting to exploit them.

- Gerald Edeh - worked on testing document and continued to meet with team and client throughout the week.

- Kolton Keller - Installed the 2021 Hac@Dac SoC on my laptop and began simulating. Started looking into building a hierarchy design diagram using an open source solution.

-Eva Kohl - Downloaded the virtual machine and learned more about the logistics of an SoC chip. Helped with the group assignment and attended team meetings.

- Savva Zeglin - Worked on the testing document. Met with team to discuss future plans for next week

- Magnus Anderson - Worked on the testing document.

What we're planning to do in the coming week

- Mason Korkowski - Getting SVLint up and running, to test against the 2018 design to find a few of the simpler bugs such as the missing default case.

- Micah Mundy - Attempting to simulate the 2018 SoC. Learn more about 2018 vulnerabilities and attempt to find similar bugs in the current SoC.

- Gerald Edeh - continue to work on team assignments and look for better understanding on the debugger.

- Kolton Keller - Find a way to build diagrams of the SoC design with open source software.

-Eva Kohl - Planning to try to uncover bugs in the SoC, work on documents, and help the team come to more concrete solutions in the current design.

- Savva Zeglin - Try to find more bugs in the SoC, and get a better understanding of what our design should look like

- Magnus Anderson - Find a bug in the 2021 SoC using manual methods. Work on starting to create a static analysis tool.

Issues we had in the previous week

- Mason Korkowski - Simply a lack of time. I did not have enough time to finish getting the Linter running.

- Micah Mundy - There is an abundance of output from the simulation. There is so much output that it has been difficult to parse.

- Gerald Edeh -had an issue with understanding the meaning of a question

- Kolton Keller - None

-Eva Kohl - Our meeting times weren’t as consistent and that made communication more difficult.

- Savva Zeglin - Just did not have enough time to get to the things I wanted to last week

- Magnus Anderson - Meeting time was at a different time than usual, wasn’t feeling great because I was sick, had another exam.